

FIG. 1

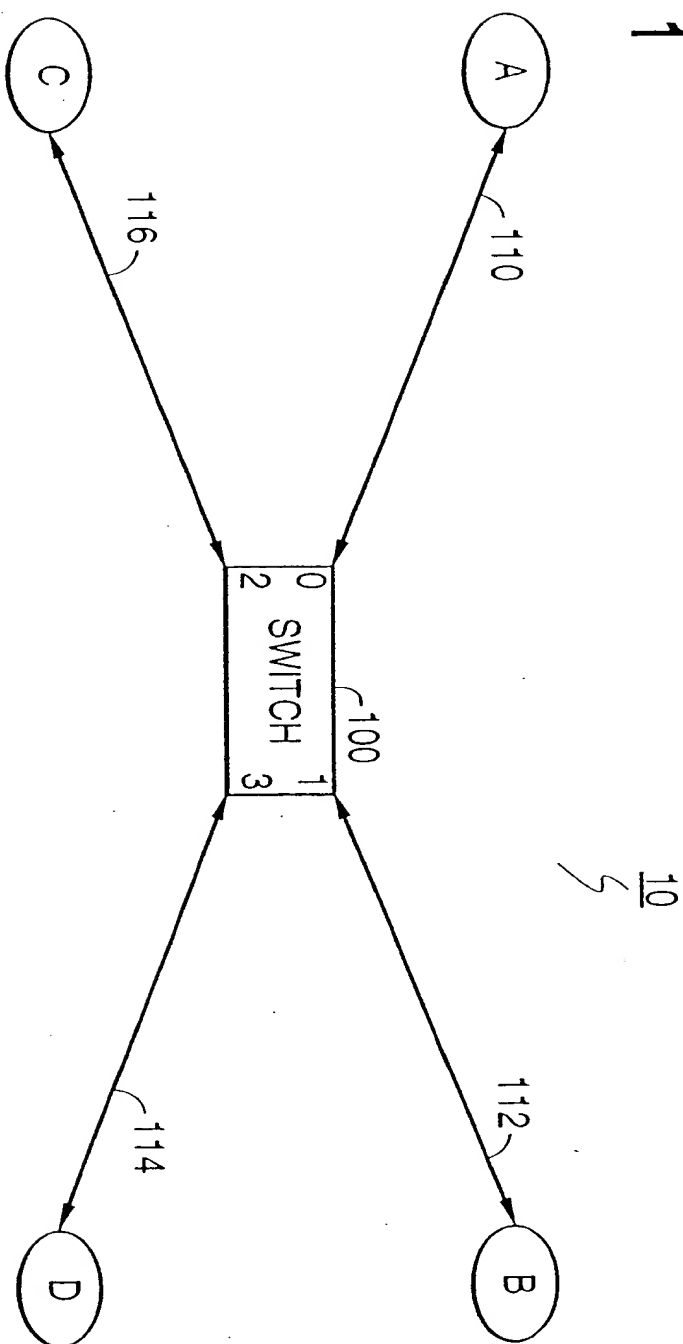


FIG. 3

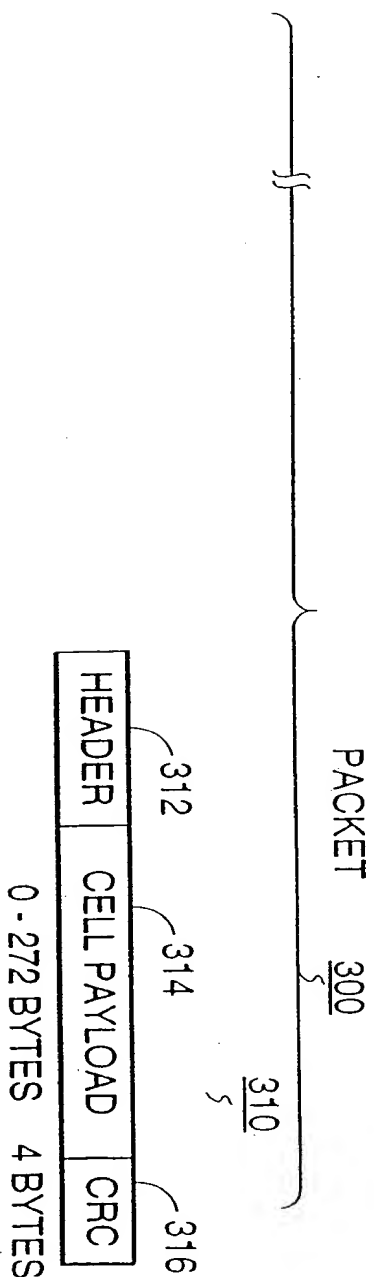
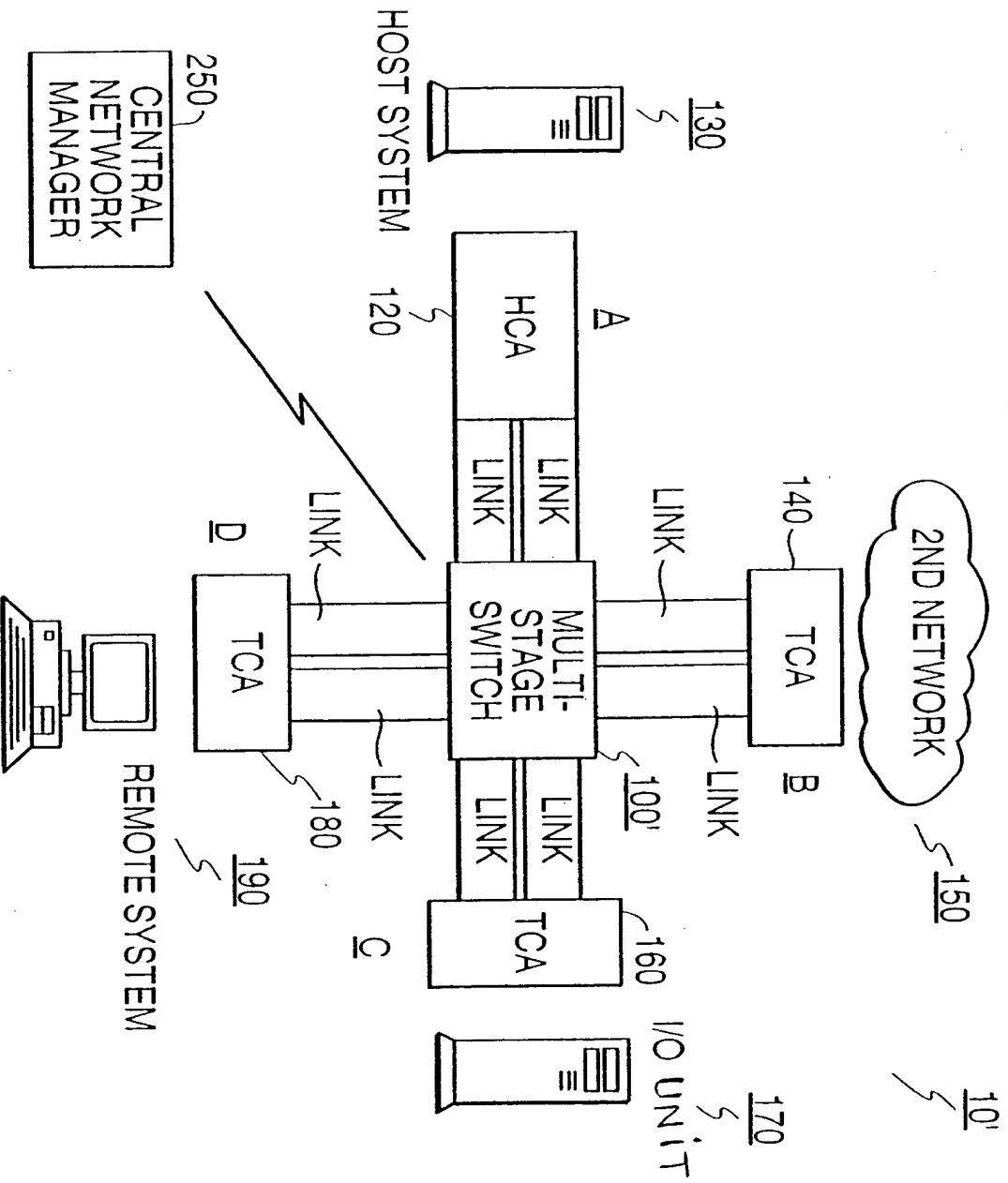


FIG. 1 is a schematic diagram of a network topology. FIG. 2 is a schematic diagram of a packet structure. FIG. 3 is a schematic diagram of a packet structure.

FIG. 2



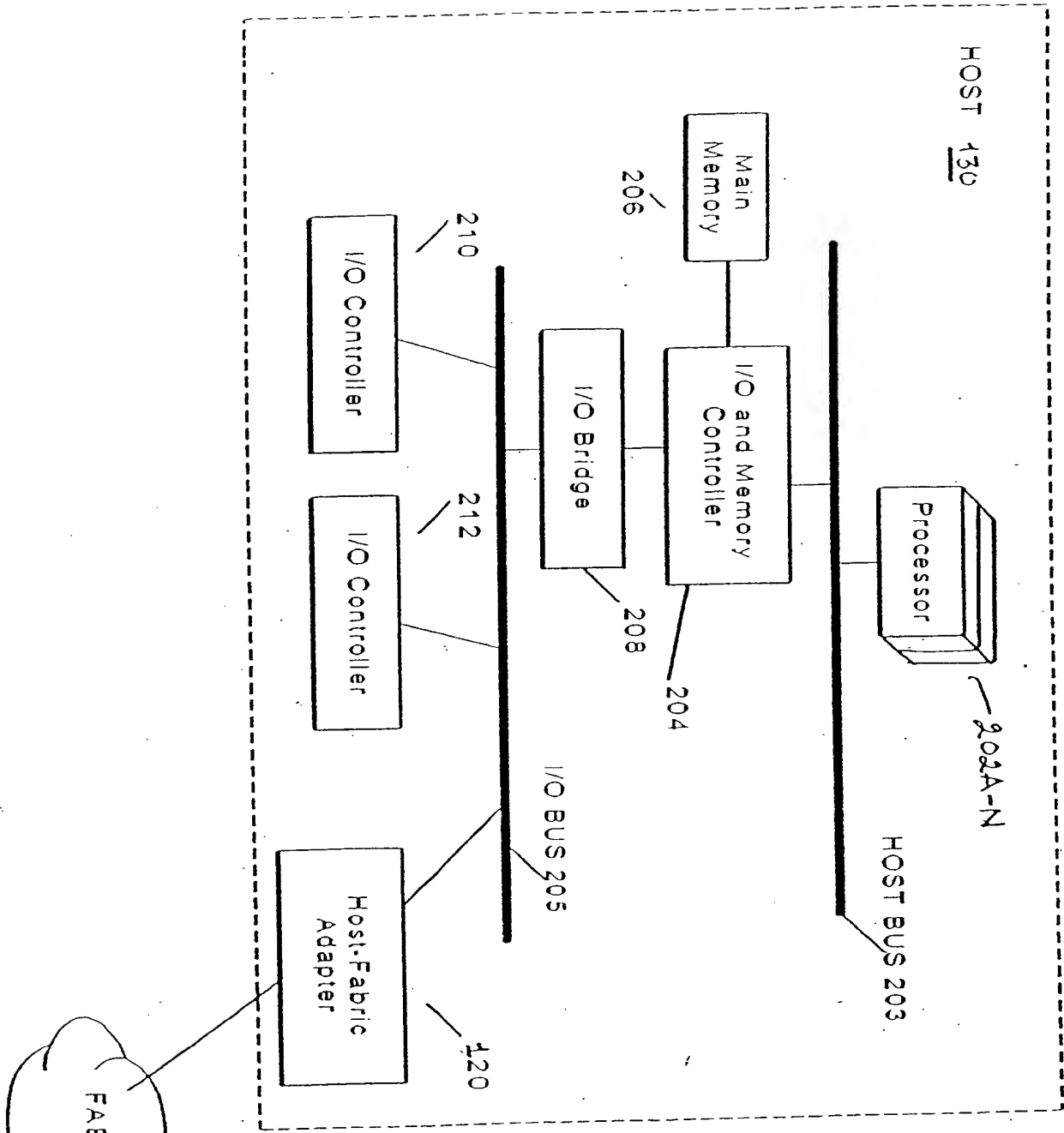


FIG. 4A

FIG. 4A is a block diagram of a host system architecture. The host system 130 includes a processor 202A-N, a host bus 203, an I/O and memory controller 204, main memory 206, an I/O bridge 208, an I/O bus 205, and I/O controllers 210, 212, and 214. The host system 130 is connected to a fabric 100 via a host-fabric adapter 420.

FIG. 4B

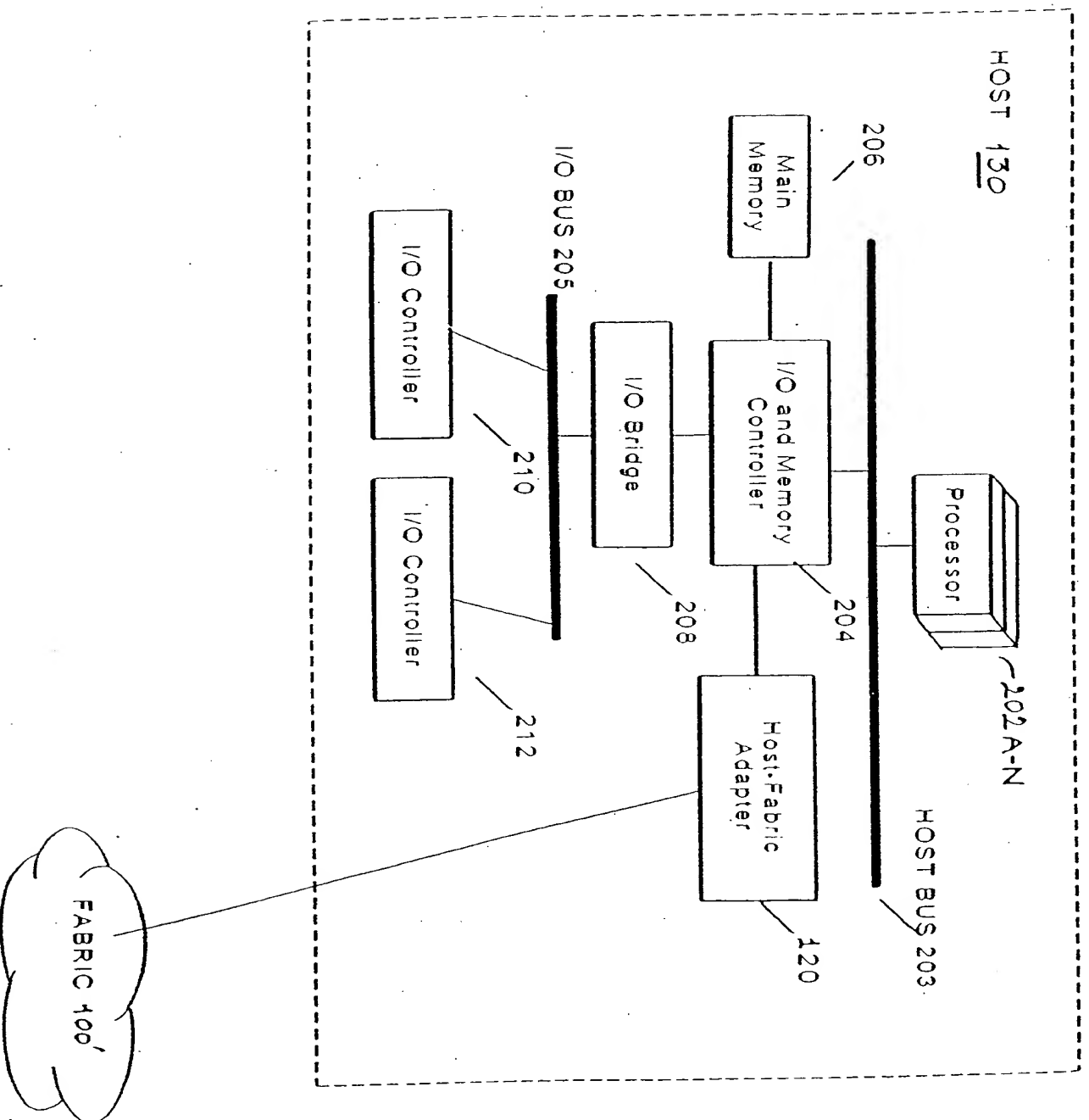
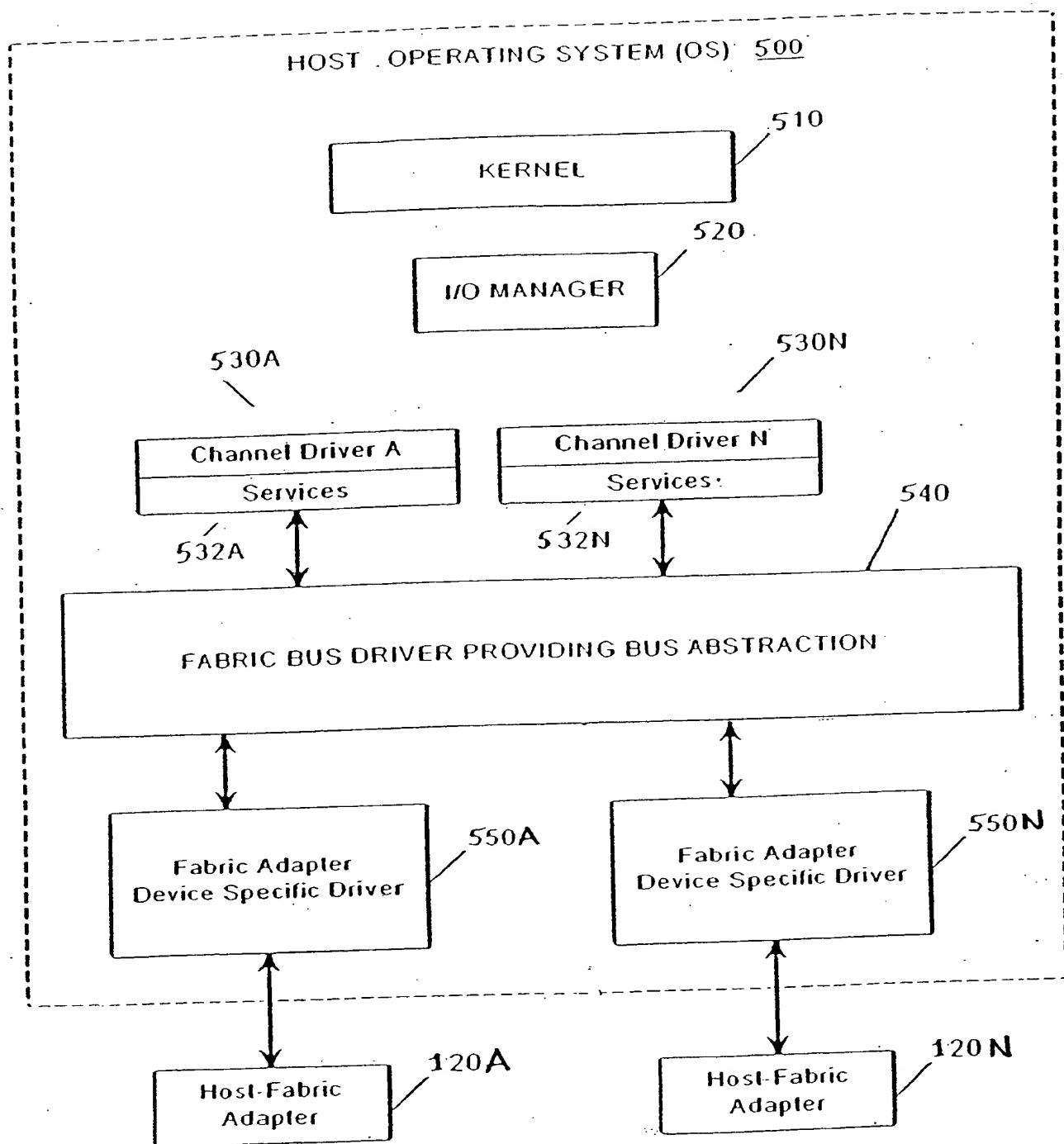


FIG. 4B is a block diagram of a host system 130, which is connected to a fabric 100'.



EXAMPLE SOFTWARE DRIVER STACKS OF HOST SYSTEM

FIG. 5

FIG. 7

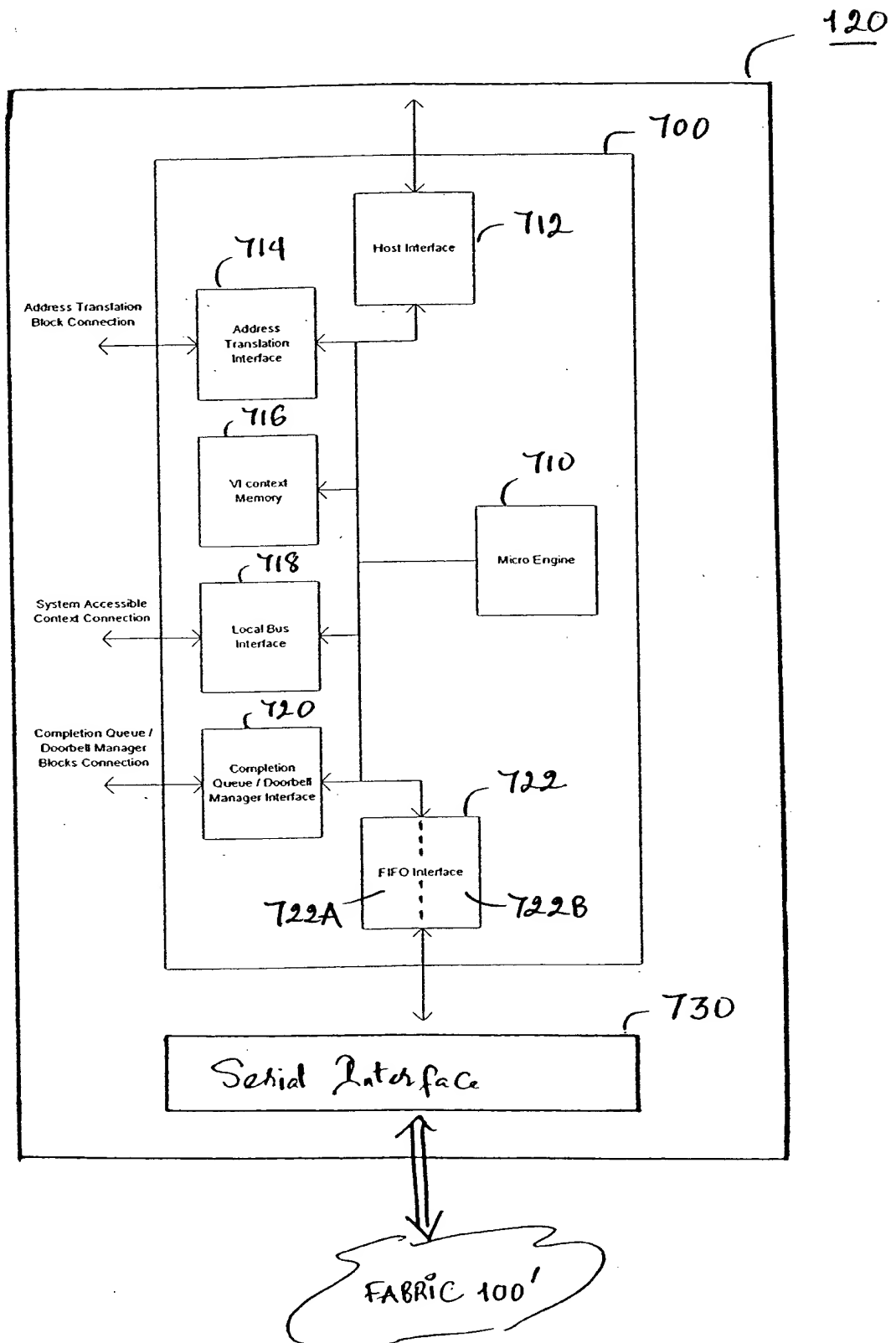


FIG. 8

710
⚡

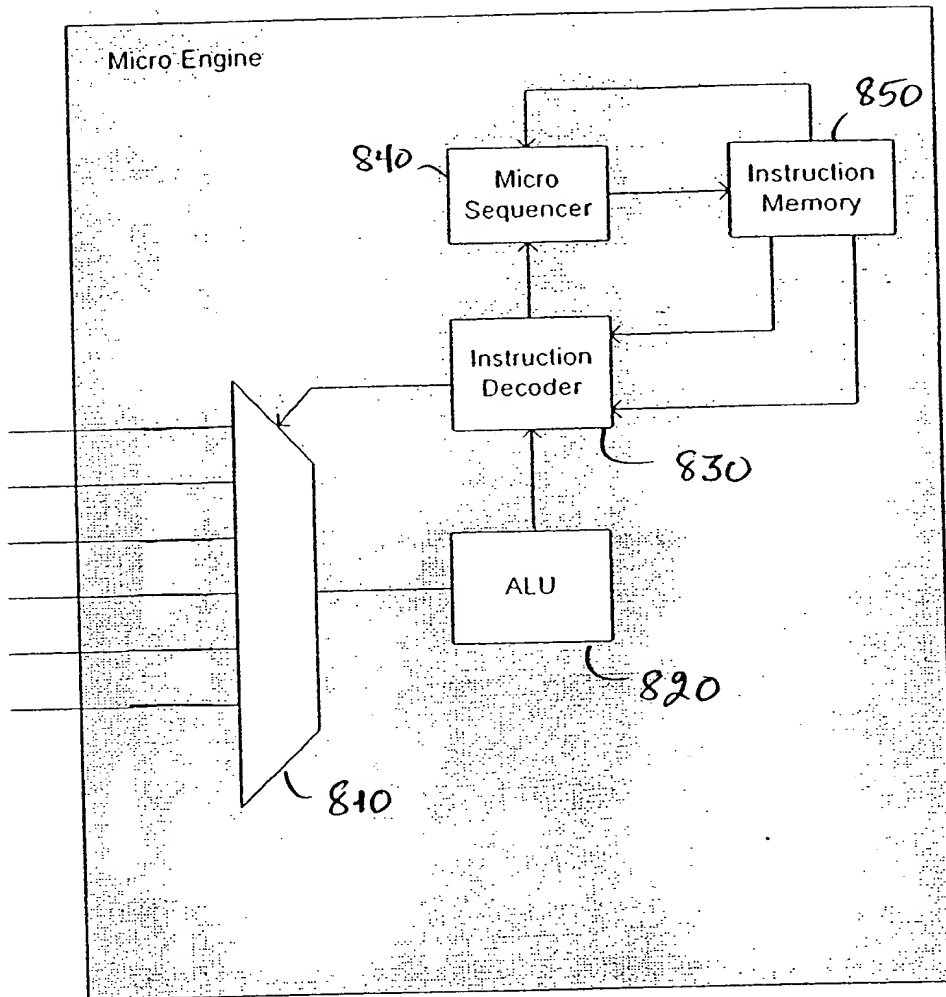


FIG. 9

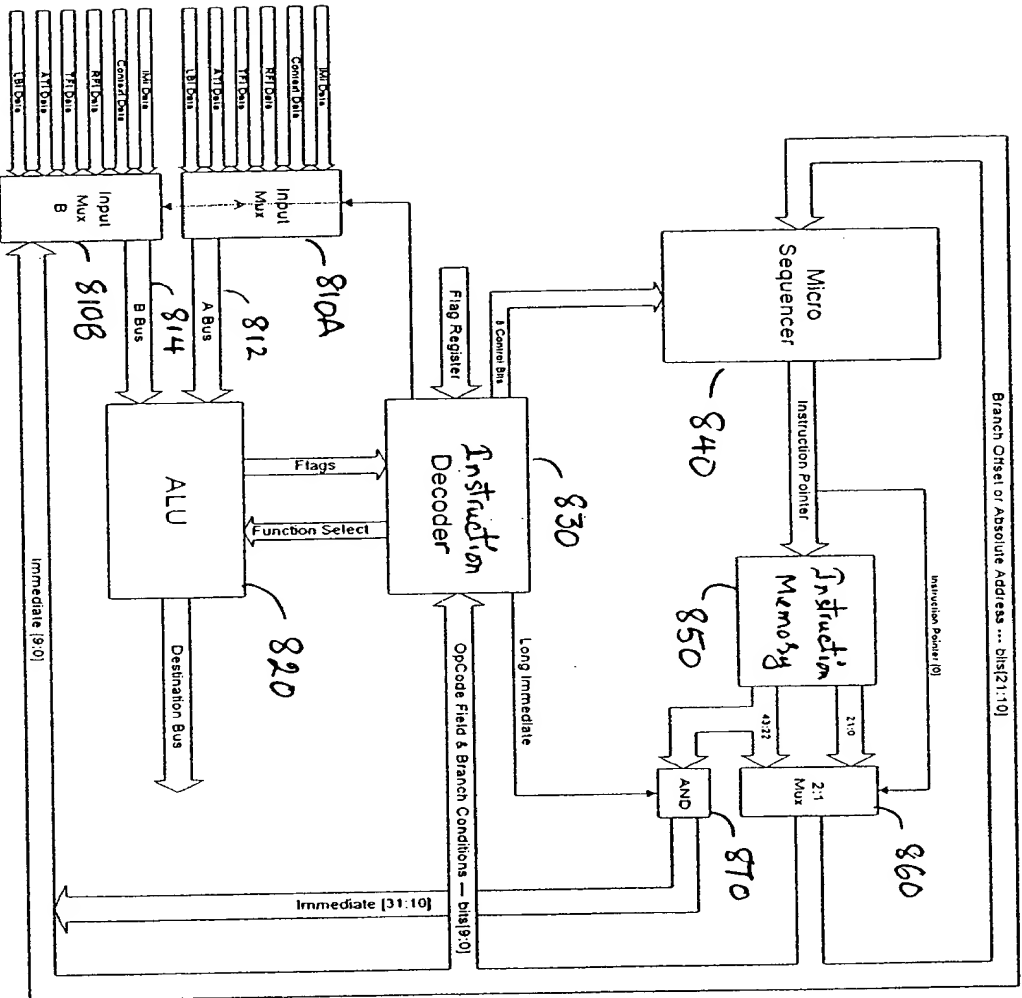
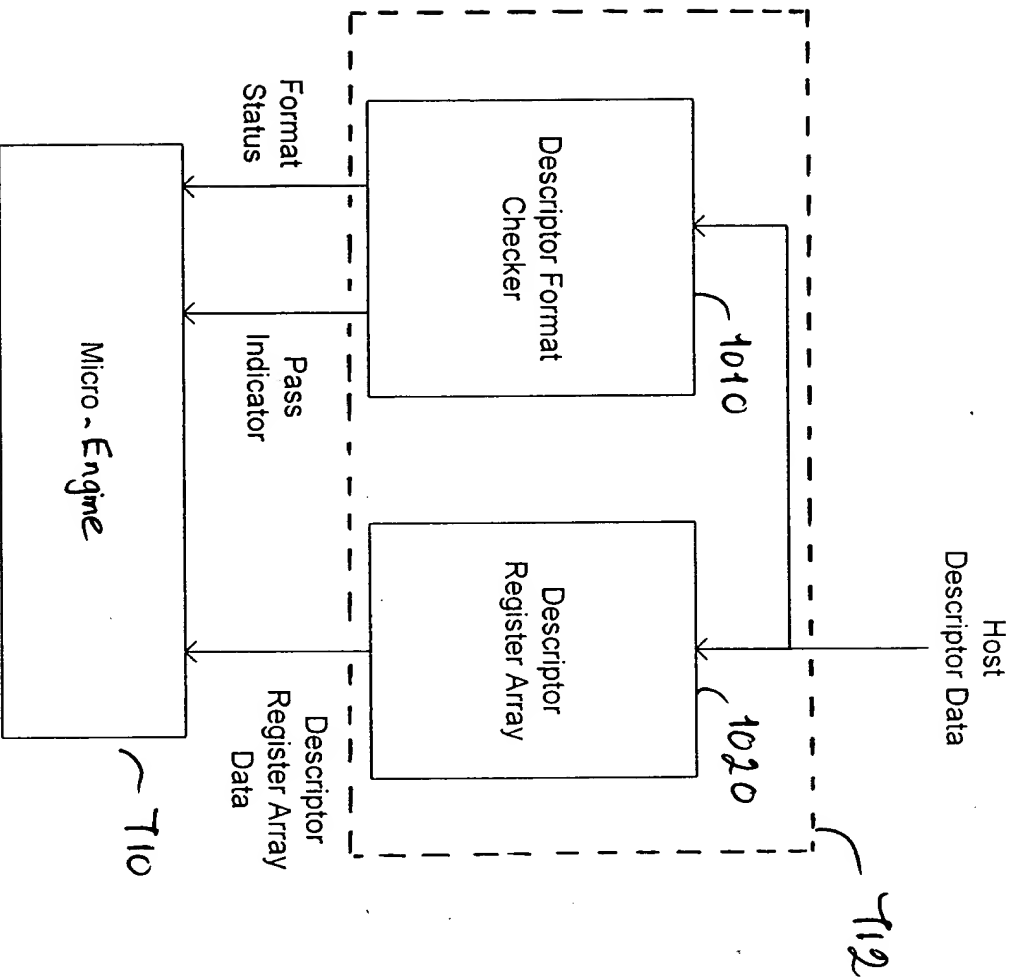


FIG. 9 is a block diagram of a processor architecture. The processor architecture includes a Micro Sequencer (840) which receives a Branch Offset or Absolute Address ... bits[21:10] and outputs an Instruction Pointer to an Instruction Memory (850). The Instruction Memory (850) outputs a 2:1 Mux (860) which provides an Instruction Pointer [0] to an Instruction Decoder (830). The Instruction Decoder (830) receives the Instruction Pointer [0] and the Long Immediate and outputs a Flag Register and a Function Select signal to an ALU (820). The Instruction Decoder (830) also outputs an Opcode Field & Branch Conditions — bits[9:0] to an AND block (870). The AND block (870) receives the Long Immediate and the Opcode Field & Branch Conditions — bits[9:0] and its output is connected to the Input Mux (812). The Input Mux (812) receives inputs from the AND block (870) and the ALU (820) and outputs to the Input Mux (810A). The Input Mux (810A) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810B) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The ALU (820) receives inputs from the Input Mux (810A) and the Input Mux (810B) and outputs a Destination Bus and a Flags signal to the Input Mux (812). The ALU (820) also outputs a Flags signal to the Input Mux (812). The Input Mux (810C) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810D) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810E) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810F) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810G) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810H) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810I) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810J) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810K) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810L) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810M) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810N) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810O) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810P) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810Q) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810R) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810S) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810T) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810U) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810V) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810W) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810X) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810Y) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Input Mux (810Z) receives inputs from the Input Mux (812) and the ALU (820) and outputs to the ALU (820). The Immediate [9:0] is connected to the Input Mux (810B) and the Input Mux (810A).

FIG. 10



1100A

1110

CONTROL SEGMENT		
LENGTH 1122	MEMORY HANDLE 1124	VIRTUAL ADDRESS 1126

1120

FIG.11A

1100B

1130

CONTROL SEGMENT		
	REMOTE MEMORY HANDLE 1142	REMOTE VIRTUAL ADDRESS 1144
LENGTH 1152	LOCAL MEMORY HANDLE 1154	LOCAL VIRTUAL ADDRESS 1156

1140

1150

FIG.11B

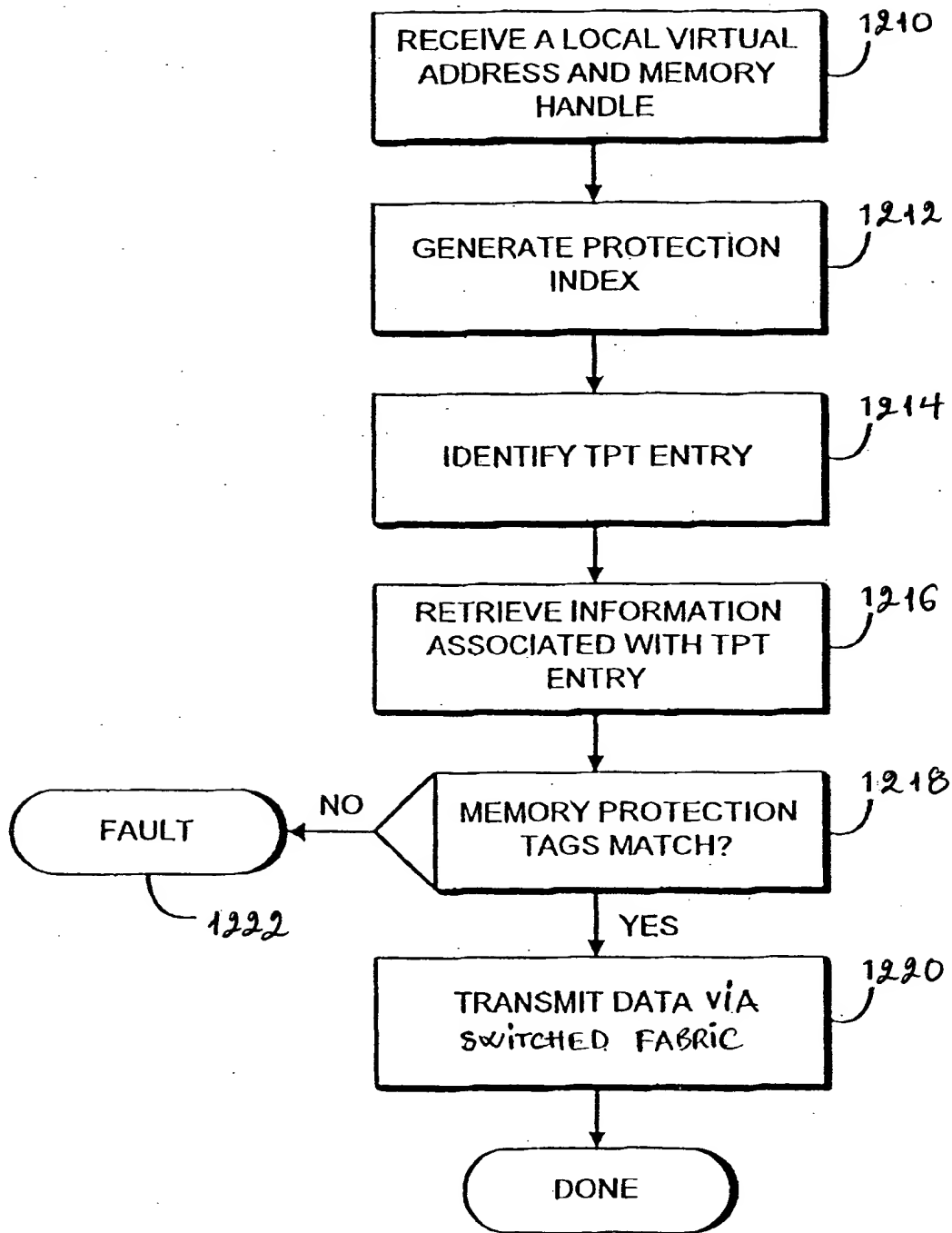


FIG. 12

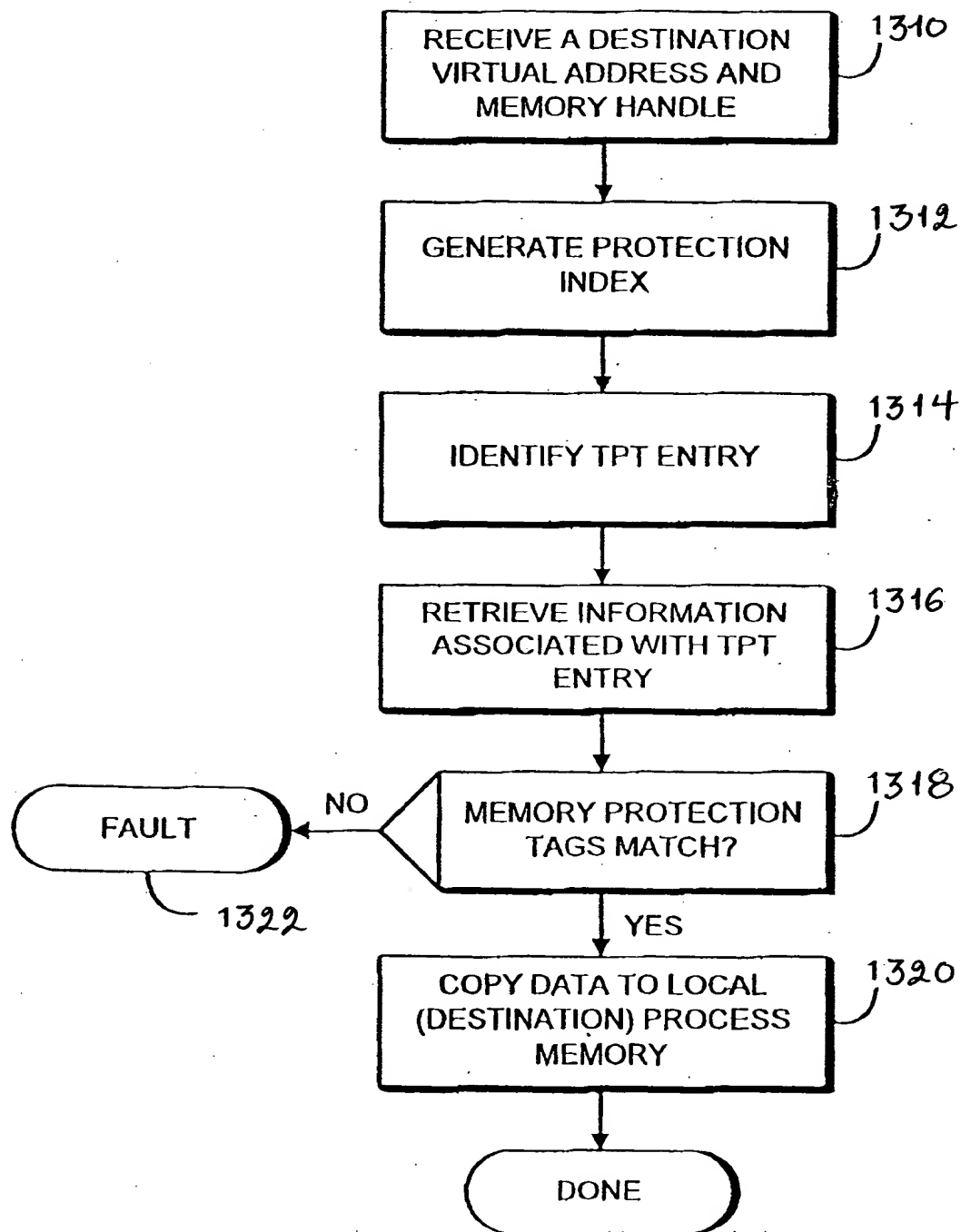


FIG. 13

FIG. 14

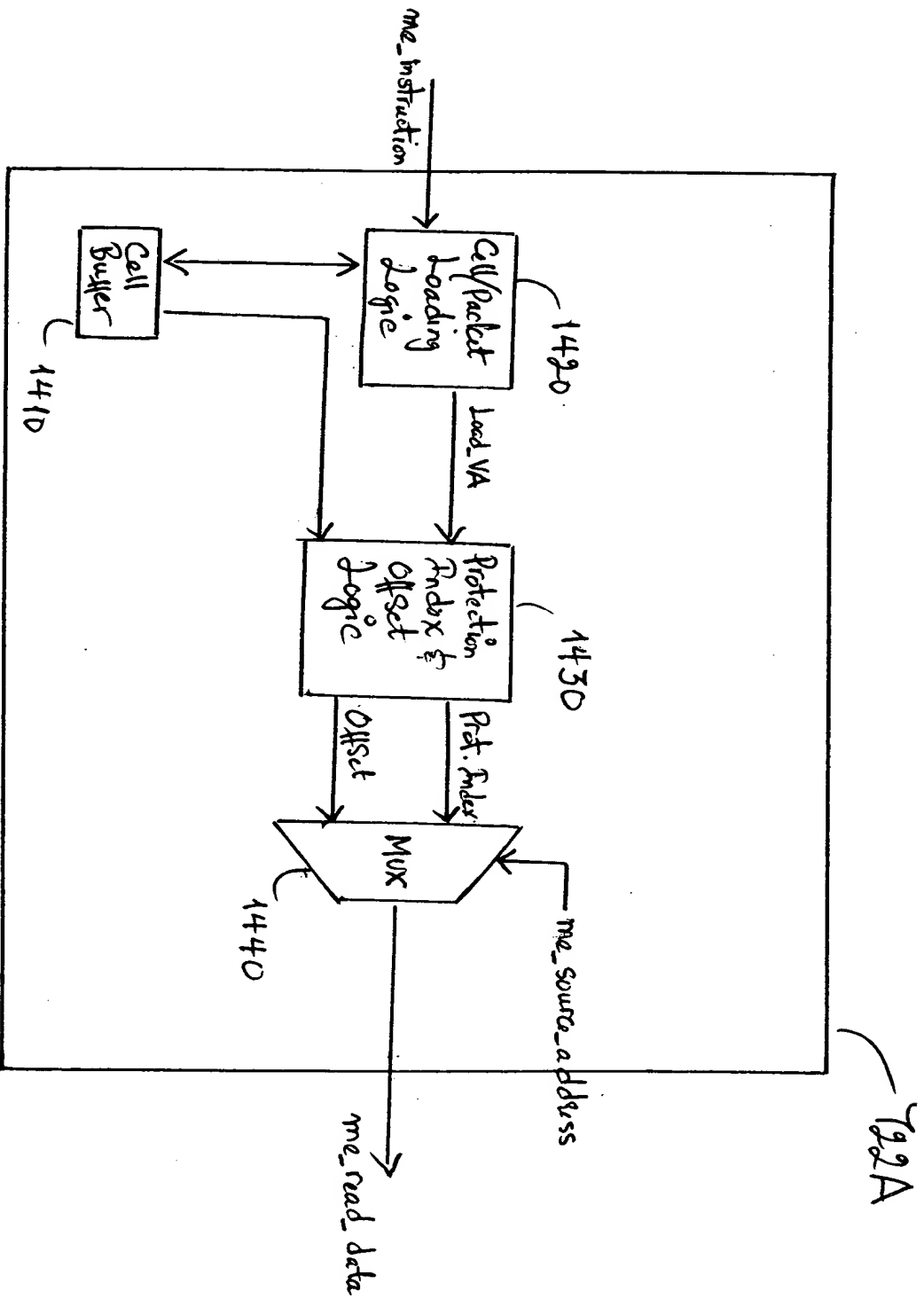


FIG. 15

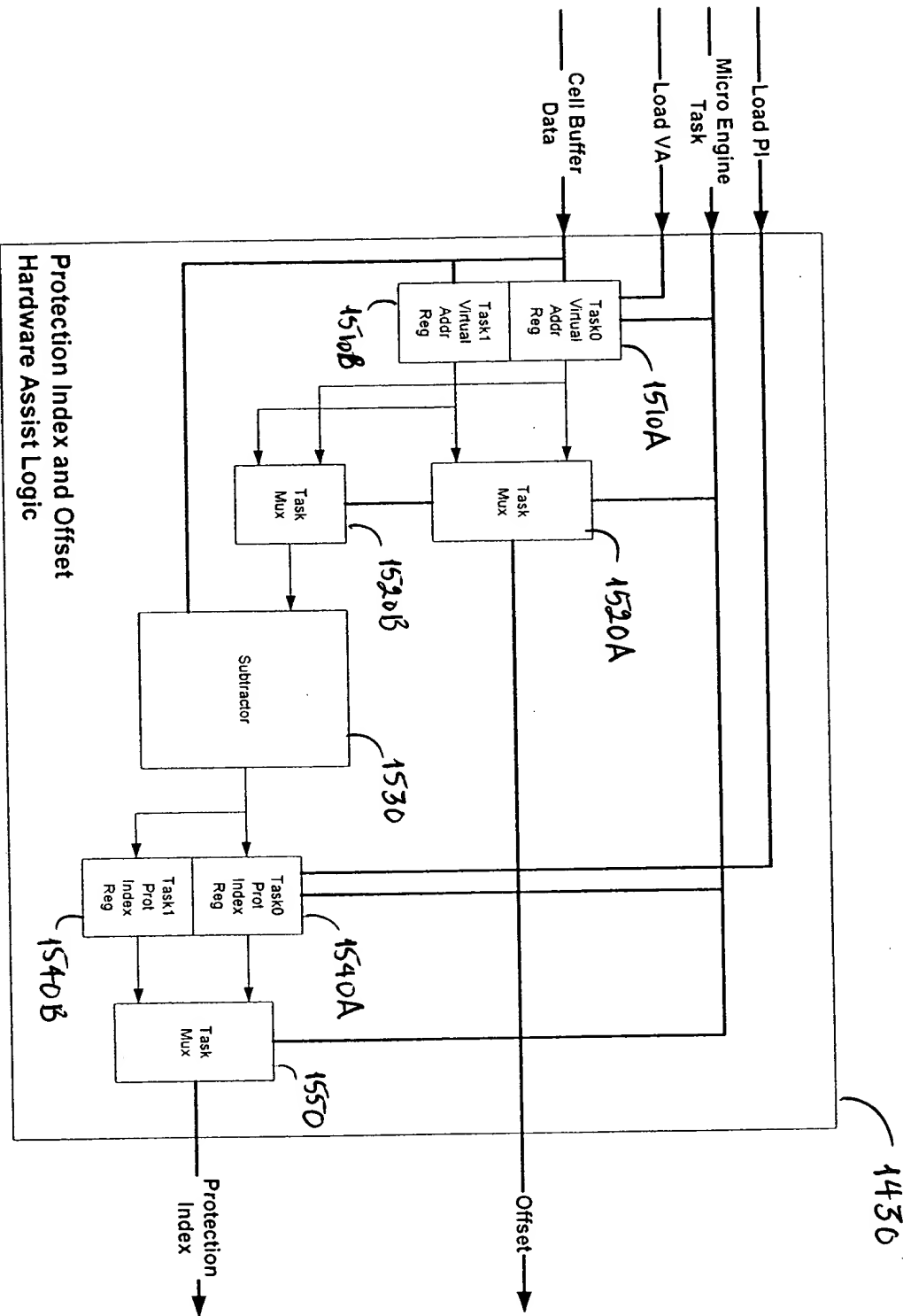
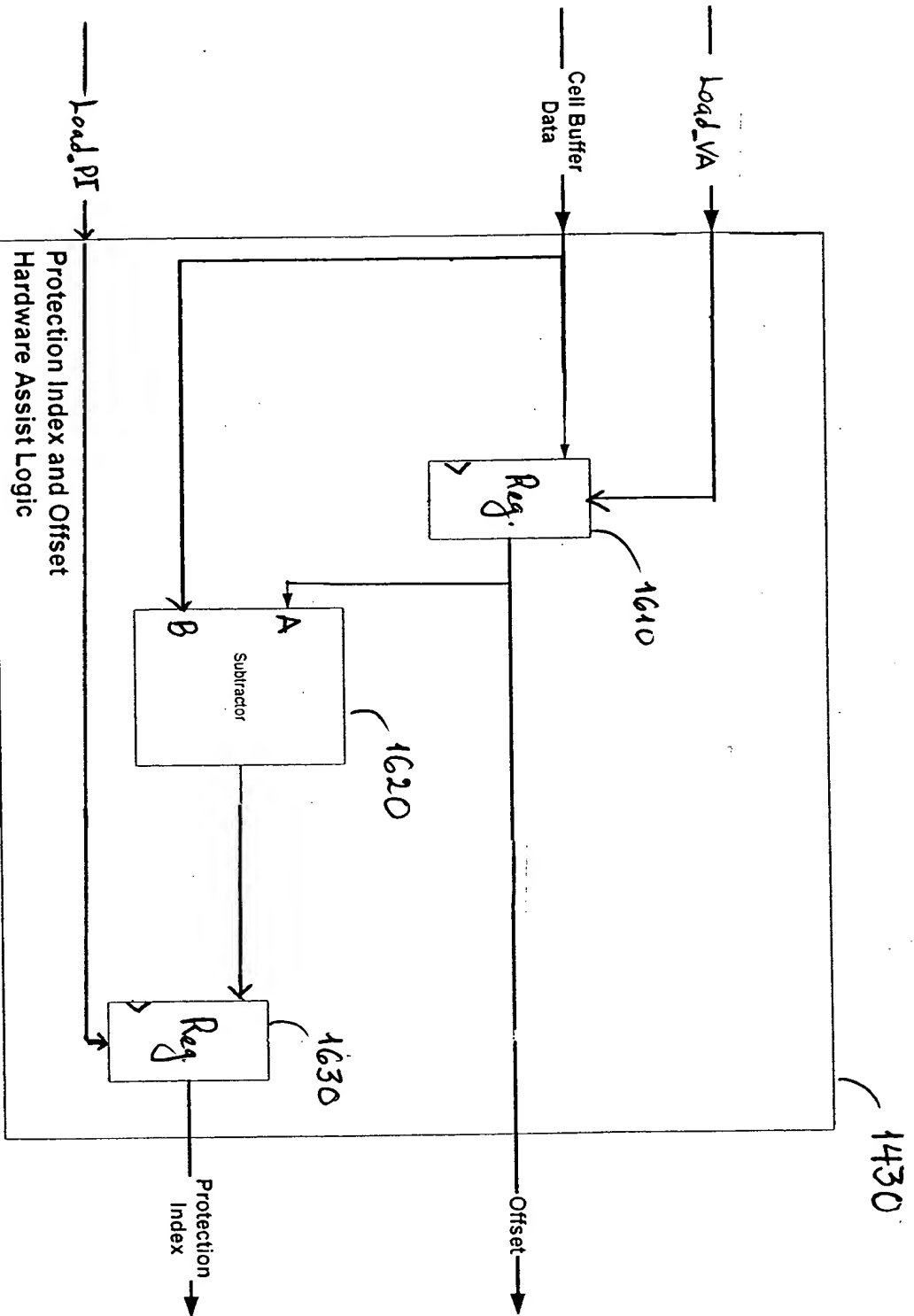


FIG. 16



FIGs. 17A-17H

FIG. 17A Clock

FIG. 17B Cell Buffer Data

FIG. 17C Load_VA

FIG. 17D Load_PI

FIG. 17E

FIG. 17F

FIG. 17G PI

FIG. 17H Offset

